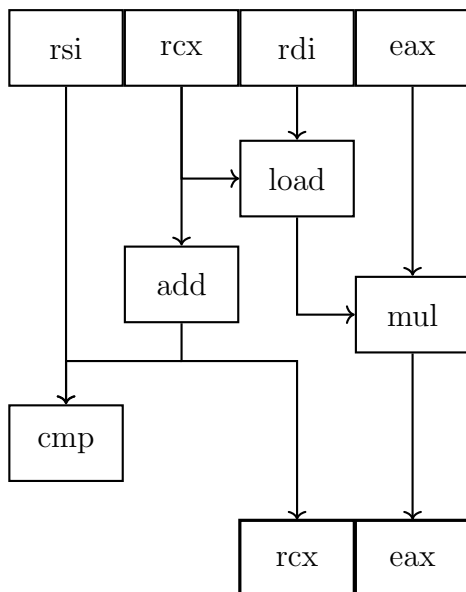


## 1. Drawing the Diagrams

For each program, create a diagram of the data dependencies.

```

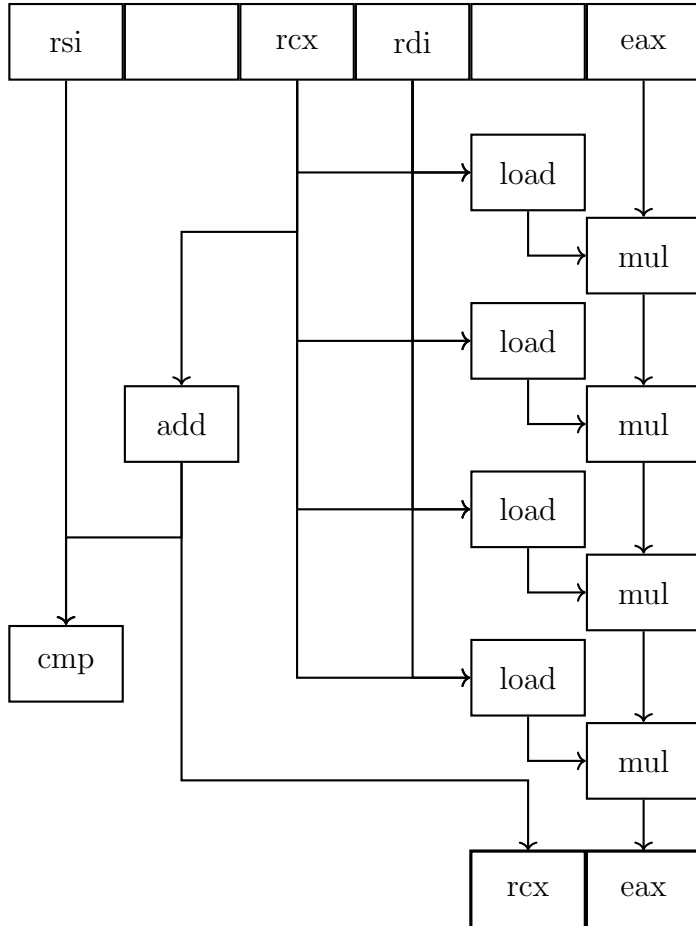
a. .L1:                                ; Loop (scalar)
    imull    (%rdi,%rcx,4), %eax        ; t = t * d[i]
    addq     $1, %rcx                  ; i++
    cmpq     %rcx, %rsi                ; Compare i:length
    jl       .L1                      ; If <, goto Loop
  
```



```

b. .L2:                                ; Loop
    imull    (%rdi,%rcx,4), %eax        ; t = t * d[i]
    imull    4(%rdi,%rcx,4), %eax      ; t = t * d[i+1]
    imull    8(%rdi,%rcx,4), %eax      ; t = t * d[i+2]
    imull    12(%rdi,%rcx,4), %eax     ; t = t * d[i+3]
    addq     $4, %rcx                  ; i += 4
    cmpq     %rcx, %rsi                ; Compare i:length
    jl       .L2                      ; If <, goto Loop

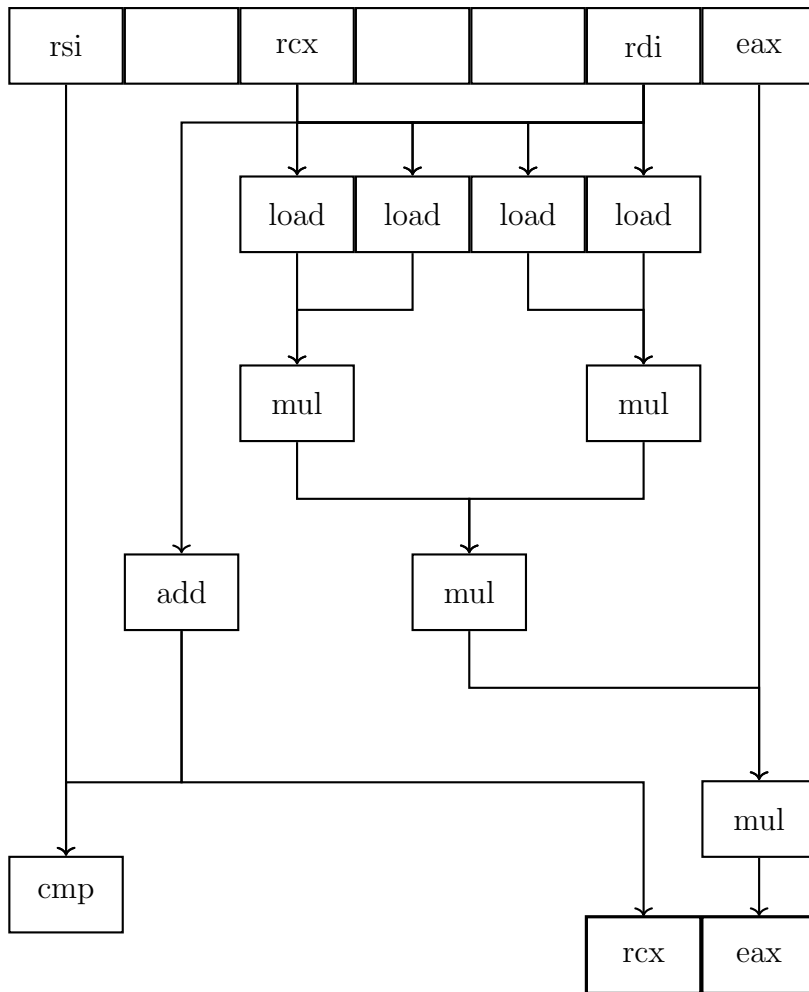
```



```

c. .L3:                                ; Loop
    mov     (%rdi,%rcx,4), %e8d        ; e8d = d[i]
    imull   4(%rdi,%rcx,4), %e8d      ; e8d = d[i+1] * d[i]
    mov     8(%rdi,%rcx,4), %e9d      ; e9d = d[i+2]
    imull   12(%rdi,%rcx,4), %e9d     ; e9d = d[i+3] * d[i+2]
    imull   %e8d, %e9d                ; e9d = e8d * e9d
    imull   %e9d, %eax                ; rax = rax * e9d
    addq    $4, %rcx                  ; i += 4
    cmpq    %rcx, %rsi                ; Compare i:length
    jl      .L3                       ; If <, goto Loop

```



## 2. Two Bounds

Given the following table for latency table:

| Instruction                  | Latency (Cycles) | Cycles/Issue | Count (#) |
|------------------------------|------------------|--------------|-----------|
| Arithmetic (except multiply) | 1                | 1            | 2         |
| Multiply                     | 2                | 2            | 4         |
| Load/Store                   | 4                | 4            | 8         |

For each prior program, provide the Cycles per Element (CPE), Throughput Bound, and Latency Bound.

For Cycles per Element,  $\max(LB, TB) / \# \text{ Elems.}$

For Latency-Bound, calculate the latency among the critical path (register to register).

For Throughput-Bound, use the formula:  $\max(\frac{(\text{Cycles/Issue}) * \text{Ops Required}}{\# \text{ Resource Count}})$  for each resource.

a. CPE: 2 Throughput: 1 Latency: 2

Throughput-Bound Calculation:

- $TB_{ALU} = \frac{1*2}{2} = 1$
- $TB_{MUL} = \frac{2*1}{4} = \frac{1}{2}$
- $TB_{LOAD/STORE} = \frac{4*1}{8} = \frac{4}{8}$
- $\max(TB_{ALU}, TB_{MUL}, TB_{LOAD/STORE}) = 1$

Latency-Bound Calculation:

- $LB = EAX \rightarrow MUL \rightarrow EAX$
- $LB = 2$

b. CPE: 2 Throughput: 2 Latency: 8

Throughput-Bound Calculation:

- $TB_{ALU} = \frac{1*2}{2} = 1$
- $TB_{MUL} = \frac{2*4}{4} = 2$
- $TB_{LOAD/STORE} = \frac{4*4}{8} = 2$
- $\max(TB_{ALU}, TB_{MUL}, TB_{LOAD/STORE}) = 2$

Latency-Bound Calculation:

- $LB = EAX \rightarrow MUL \rightarrow MUL \rightarrow MUL \rightarrow MUL \rightarrow EAX$
- $LB = 8$

c.

CPE: .5

Throughput: 2

Latency: 2

Throughput-Bound Calculation:

- $TB_{ALU} = \frac{1*2}{1} = 2$
- $TB_{MUL} = \frac{2*4}{4} = 2$
- $TB_{LOAD/STORE} = \frac{4*4}{8} = 2$
- $\max(TB_{ALU}, TB_{MUL}, TB_{LOAD/STORE}) = 2$

Latency-Bound Calculation:

- $LB = EAX \rightarrow MUL \rightarrow EAX$
- $LB = 2$